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SHAW PITTMAN
IP GROUP
1650 TYSONS BOULEVARD
SUITE 1300
MCLEAN, VA 22102

EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,945	HORIE, YOSHITAKA	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 05/07/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 1, 22 and 23 are objected to because of the following informalities: Claim 1, line 8 (or claim 22, line 8; or claim 23, line 8), the phrase "respective materials" fails to clarify what are materials. The phrase should be changed to "respective solder materials". Appropriate correction is required.

Claim 1 is objected to because of the following informalities: Claim 1, lines 12-13 (or claim 22, lines 10-11; or claim 23, lines 10-11), the phrase "wherein the first solder material is caused to solidify earlier than the second solder material..." fails to reflect the subject matter of the instant invention as to why the first solder material solidifies earlier than the second solder material. The phrase should be changed to "wherein the first solder material has a melting temperature higher than that of the second solder material and is caused to solidify earlier than the second solder material...". Appropriate correction is required.

Claim 22 is objected to because of the following informalities: Claim 22, lines 12-13 (or claim 23, lines 12-13), the phrase "wherein the heating of the first solder material is terminated earlier than the heating of the second solder material" is not fully described the subject matter of the instant invention as to why the first solder material is terminated earlier than the second solder material. The phrase should be changed to "heating of the first and the second solder materials is performed by contacting the lower and the upper conductors with first and second heaters, respectively; and wherein the heating of the first solder material is terminated earlier than the heating of the second solder material". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,005,454 to Froloff et al. in view of US Patent No. 5,888,850 to Havens et al.

Froloff et al. (figure 1) teach a method of making a semiconductor device, the method comprising the steps of: mounting a semiconductor chip (1) on a lower conductor (8), with first solder material (10) applied between the chip (1) and the lower conductor (8); positioning an upper conductor (7) on the chip (1), with second solder material (9) applied between the chip (1) and the upper conductor (7) (column 3, line 22-column 4, line 35);

wherein the lower conductor (8) includes a die pad portion (6) for mounting the semiconductor chip (1); and

since each of the first and second solder materials (10, 9) can be one of the lead (Pb) and tin (Sn) alloy, the second solder material [9] can be tin alloy and the first solder material [10] can be lead.

Froloff et al. differ from the claimed invention by not showing heating up the first and second solder materials beyond melting points of the respective solder materials; solidifying the first and the second solder materials; and wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step for securing the semiconductor chip

on the die pad portion of the lower conductor is fixedly connected to the semiconductor chip. However, Havens et al. (column 8, line 55 – column 9, line 5) teach heating up the first and second solder materials beyond melting points of the respective solder materials; and solidifying the first and the second solder materials; and wherein the first solder material is caused to solidify earlier than the second solder material. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Havens et al. into the device taught by Froloff et al. because it keeps the required precise electrical connecting between the semiconductor chip and the other devices. The combined device shows the first solder material is caused to solidify earlier than the second solder material in the solidifying step for securing the semiconductor chip on the die pad portion of the lower conductor is fixedly connected to the semiconductor chip.

Regarding claim 2, the combined device shows the melting point of the first solder material is higher than the melting point of the second solder material.

Regarding claim 3, the combined device shows the first solder material has a melting temperature higher than the second solder material, so that the heating of the first solder material is terminated earlier than the heating of the second solder material.

Regarding claim 22, the disclosures of Froloff et al. and Havens et al. are discussed as applied to claims 1-3 above.

5. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Froloff et al. in view of Havens et al. as applied to claims 1-3 above, and further in view of US Patent No. 4,920,574 to Yamamoto et al.

The disclosures of Froloff et al. and Havens et al. are discussed as applied to claims 1-3, Froloff et al. and Havens et al. differ from the claimed invention by not showing the heating of the first and the second solder material is performed by contacting the lower and the upper conductors with first and second heaters, respectively. However, Yamamoto et al. teach the heating of the solder material with the heaters (see figures 13,15 -16; column 9, lines 60-65; column 10, line 47 – column 11, line 1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamamoto et al. into the device taught by Froloff et al. because the heaters are conventional electric heater for melting the solder material.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Froloff et al. in view of Havens et al. as applied to claims 1-3 above, and further in view of Applicant's Admitted Prior Art (AAPA).

The disclosures of Froloff et al. and Havens et al. are discussed as applied to claims 1-3, Froloff et al. differ from the claimed invention by not showing a semiconductor chip includes a protruding upper electrode being connected to the upper conductor. However, AAPA (figures 18-19) teaches a semiconductor chip (90) includes a flat lower electrode (90a) and a protruding upper electrode (90b), the lower electrode (90a) being connected to the lower conductor and the upper electrode (90b) being connected to the upper conductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of AAPA into the device taught by Froloff et al. for better connection between the upper electrode and the chip.

7. Claims 6-8 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Froloff et al. in view of Havens et al. as applied to claims 1-3 above, and further in view of US Patent No. 4,994,412 to Kalfus et al.

The disclosures of Froloff et al. and Havens et al. are discussed as applied to claims 1-3, Froloff et al. and Havens et al. differ from the claimed invention by not showing the step of preparing a conductive frame, which includes the lower and the upper conductors. However, Kalfus et al. (figures 5 and10) teach a conductive frame (120), which includes the lower and the upper conductors (12, 13, 50, 60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a conductive frame, which includes the lower and the upper conductors, of Kalfus et al. into Froloff et al. and Havens et al. because the lead frame is a well known structure for supporting the semiconductor device and providing connection between the external device and semiconductor device.

Regarding claim 7, the combined device shows the lower conductor comprises a die pad portion and lower lead portions extending from the die pad portion, the semiconductor chip being mounted on the die pad portion.

Regarding claim 8, the combined device shows the upper conductor comprises upper lead portions.

Regarding claim 17, Froloff et al. and Havens et al. differ from the claimed invention by not showing a step of preparing a conductive frame, which includes a first conductive pattern and a second conductive pattern, the first conductive pattern including the lower conductor, the second conductive pattern including the upper conductor. However, Kalfus et al. (figure 10)

teach a step of preparing a conductive frame (120), which includes a first conductive pattern (12, 13) and a second conductive pattern (50, 60), the first conductive pattern (12, 13) including the lower conductor, the second conductive pattern (50, 60) including the upper conductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kalfus et al. into the device taught by Froloff et al. and Havens et al. because conductive frame is a well known structure in the art for supporting the semiconductor device and providing connection between the semiconductor device and the external device.

Regarding claim 18, the combined device shows the lower conductor further comprises lower lead portions extending from the die pad portion.

Regarding claim 19, the combined device shows the second conductive pattern comprises upper lead portions at least one of which is to be connected to the semiconductor chip as the upper conductor.

Regarding claim 20, Froloff et al., Havens et al. and Kalufs et al. differs from the claimed invention by not showing the step of removing at least one of the lower and the upper lead portions from the frame. It would have been obvious to one having ordinary skill in the art at the time the invention was made for removing at least one of the lower and the upper lead portions from the frame because the portion of the lead frame must be cut in the final step for separating the lead finger from each other. It is known in the art as shown for example by US Patent No. 6,307,755 to Williams et al. (figures 18F-G).

Regarding claim 21, the combined device shows the frame comprises first and second common bars parallel to each other, the upper lead portions being divided into first and second

group, the upper lead portions in the first group extending from the first common bar toward the second common bar, the upper lead portions in the second group extending from the second common bar toward the first common bar.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Froloff et al. in view of Havens et al. as applied to claims 1-3 above, and in view of Kalfus et al. as applied to claims 6-8 and 17-21 above, and further in view of US Patent No. 4,980,568 to Merrick et al.

The disclosures of Froloff et al., Havens et al. and Kalfus et al. are discussed as applied to claims 1-3, 6-8 and 17-21 above, Froloff et al.. Havens et al. and Kalfus et al. differ from the claimed invention by not showing the step of rotating the upper conductor about an axis relative to the lower conductor, so that the upper conductor comes into facing relation to the lower conductor. However, Merrick et al. (figure 2) teach to rotate the upper lead to a position over the lower lead (column 4, lines 40-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merrick et al. into the device taught by Froloff et al., Havens et al. and Kalfus et al. because it provides a fixed spacing between the upper and lower leads. The combined device shows the step of rotating the upper conductor about an axis relative to the lower conductor, so that the upper conductor comes into facing relation to the lower conductor.

Response to Arguments

9. Applicant's arguments with respect to claims 1-8, 11 and 17-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
July 25, 2003

SHOUXIANG HU
PRIMARY EXAMINER